Design and Performance of Monolithic GaAs Direct-Coupled Preamplifiers and Main Amplifiers

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Abstract—**The design and performance of a GaAs direct-coupled preamplifier and main amplifier is described. The amplifiers are fabricated by the self-aligned implantation for n^+-layer technology (SAINT) process. The developed preamplifiers have 13-dB gain, 3-GHz bandwidth, and 4.8-dB noise figure for the one-stage amplifier, and 22-dB gain, 2.7-GHz bandwidth, and 5.6-dB noise figure for the two-stage amplifier. The developed four-stage main amplifier has 36-dB gain and 1.5-GHz bandwidth with a power consumption of 710 mW. These amplifiers are promising candidates for application to high-speed data communication systems.**

I. Introduction

OVER THE LAST decade, GaAs FET's have established a solid basis in microwave systems. Moreover, recent advances in GaAs IC technology have made it possible to develop large-scale integration of GaAs FET circuits [1].

Due to their small integration scale, GaAs analog IC's are the nearest candidates for practical application among these IC's. In the analog IC's, monolithic broad-band amplifiers are needed because of their wide applications such as mobile, satellite, and high-speed data communication systems. Therefore, various kinds of amplifiers have been studied [2]–[4]. Among these amplifiers, the direct-coupled amplifiers first reported by D. P. Hornbuckle *et al.* [3], which made use of only FET's, diodes, and resistors, have the advantage of broad bandwidth from dc frequency, small chip sizes, and easy integration with the digital circuits.

For high-speed data communication systems, a low-noise, low-VSWR, and high-gain amplifier is required. Previously reported high-gain direct-coupled amplifiers had multistage constructions with their gain ranging from 26 dB to 42 dB [5], [6]. However, these amplifiers are not necessarily adequate for the above purpose because they were designed for general purpose use. For example, because they consisted of common-gate FET's in the input stages, their noise figure was not enough low (about 9 dB with a 248-μm gate-width FET). Moreover, the bandwidth degradation between the stages, which is important for a multistage amplifier, was not discussed.

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In this paper, the circuit configurations which are suitable for a low-noise and low-VSWR preamplifier and a high-gain main amplifier are presented, followed by the design considerations including noise figure, input VSWR, and multistage connection. For a preamplifier, a common-source configuration with a resistive feedback from a source-follower stage is newly presented. The amplifiers are fabricated by the self-aligned implantation for n^+-layer technology (SAINT) process [7]. The developed preamplifiers have 13-dB gain, 3-GHz bandwidth, and 4.8-dB noise figure for a one-stage amplifier, and 22-dB gain, 2.7-GHz bandwidth, and 5.6-dB noise figure for two-stage amplifier. The developed four-stage main amplifier has 36-dB gain and 1.5-GHz bandwidth with a power consumption of 710 mW. These amplifiers are promising candidates for applications to high-speed data communications systems.

II. FET Model for the Circuit Design

An equivalent circuit and drain current equations used for the circuit design are shown in Fig. 1(a). Drain current I_D was described in a modified SPICE form [8]. FET parameters used for the circuit design are listed in Table I. The parameters of β, γ, and λ were determined by fitting the drain I–V characteristics. Gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} were derived from the change of the charges in the depletion layer under the FET gate [8]. Source resistance R_s and drain resistance R_d were estimated by the gate-to-source and gate-to-drain diode characteristics. Gate resistance R_g was calculated from the gate dimensions.

An equivalent circuit for noise analysis is shown in Fig. 1(b). Noise sources $\langle i_{nrj}^2 \rangle$ ($j = g$, s, and d) and $\langle i_{nd}^2 \rangle$ represent the thermal noise of R_g, R_s, R_d, and drain current noise, respectively. The factor P for the drain current noise form depended on an FET structure. Therefore, in the noise calculations, it was necessary to vary P for fitting experimental results. Gate-induced noise was neglected in the present work because it was small in the frequencies below the cutoff frequency.

Noise-figure (NF) dependencies on transconductance g_m were calculated for comparison with the experimental values. The value of factor P was assumed to be either 2/3, 1, or 2. The noise figure of an FET with a threshold voltage of -1 V and a gate dimension of 1 μm$\times$150 μm was

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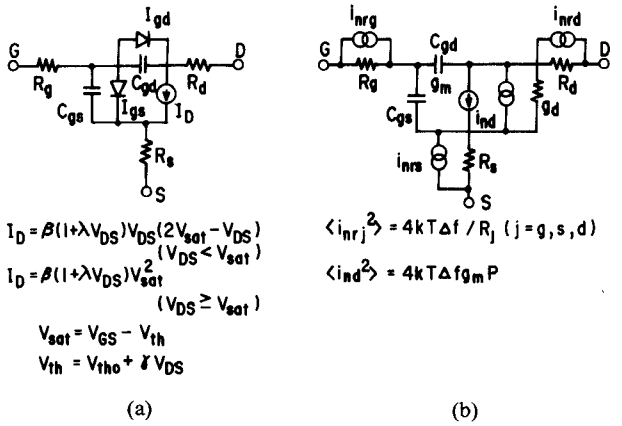


Fig. 1. FET models used for the circuit design. (a) FET model. A drain current I_D is described by the modified SPICE form with the fitting parameters β, γ, and λ. (b) FET noise model. $\langle i_{nrj}^2 \rangle$ and $\langle i_{nd}^2 \rangle$ represent thermal noise sources of R_g, R_s, and R_d, and drain current noise source, respectively. P is the fitting parameter for the drain current noise.

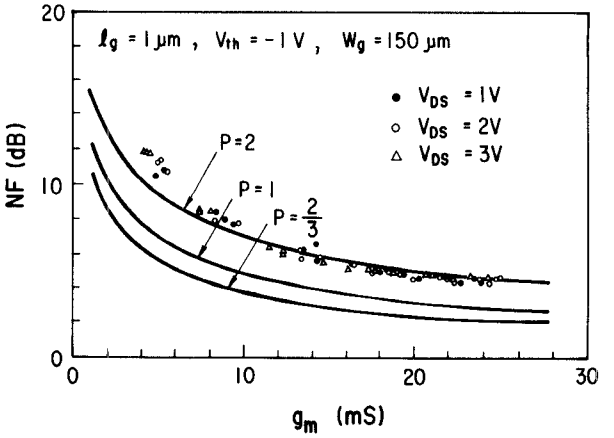
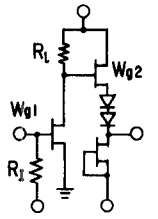
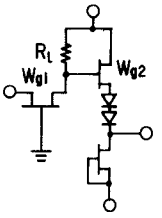
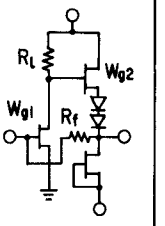


Fig. 2. Noise figure (NF) dependencies on transconductance g_m. ●○△: Experimental results. ——: Calculated results. Noise figure was evaluated at 1 GHz for 50-Ω signal source impedance.

TABLE I
FET PARAMETERS USED FOR THE CIRCUIT DESIGN

NAME	SYMBOL	TYPICAL VALUE	CONDITION
Transconductance parameter	β	0.064 A/V²/mm	——
Channel thickness modulation parameter	γ	0.05	——
Channel length modulation parameter	λ	0	——
Threshold voltage	V_{th}	-1.0V	V_{DS} = 2V
Gate length	ℓ_g	1.0 μm	——
Transconductance	g_m	110mS/mm	V_{DS} = 2V V_{GS} = 0V
Drain conductance	g_d	7mS/mm	V_{DS} = 2V V_{GS} = 0V
Source resistance	R_s	0.5 Ω·mm	——
Drain resistance	R_d	0.5 Ω·mm	——
Gate resistance	R_g	0.6 Ω	W_g = 100 μm W_{gf} = 50 μm
Gate-to-source capacitance	C_{gs}	1.1 pF/mm	V_{DS} = 2V V_{GS} = 0V
Gate-to-drain capacitance	C_{gd}	0.1 pF/mm	V_{DS} = 2V V_{GS} = 0V

TABLE II
LOW-VSWR DIRECT-COUPLED AMPLIFIERS WITH SIMPLIFIED FORMS OF THEIR NOISE FIGURE NF AND INPUT IMPEDANCE Z_{in}

	(a)	(b)	(c)
Circuit			
NF	$1+\frac{R_{ss}}{R_I}+\frac{P}{g_m R_{ss}}\left(\frac{R_{ss}+R_I}{R_I}\right)^2$	$1+\frac{P}{g_m R_{ss}}$	$1+\frac{R_{ss}}{R_f}+\frac{P}{g_m R_{ss}}$
Z_{in}	R_I	$\frac{1}{g_m}$	$\frac{1+g'_m R_f}{g'_m (g_m R_L+1)}$

R_{ss}: Signal-source impedance. g_m: Transconductance of input FET. g'_m: Transconductance of source-follower FET.

measured at 1 GHz for a 50-Ω signal-source impedance. The calculated values and measured ones are shown in Fig. 2. The experimental results are located around the calculated curve whose P was 2. Therefore, it was found possible to design the noise figure of the amplifiers using the appropriate value of P.

III. CIRCUIT DESIGNS

All designs were based on computer simulations, with either ASTAP or SPICE, using the FET models mentioned above. In noise calculations, P was ranged from 2/3 to 2 to obtain general results.

A. A Preamplifier

Low noise and low VSWR, as well as broad bandwidth, were required for the preamplifier. From this point of view, optimum preamplifier circuit construction was studied. Table II shows three kinds of direct-coupled and low-VSWR amplifiers with the simplified forms of their noise figure and input impedance. Circuit (a) consists of a common-source FET with a matching resistor R_I parallel to the input port. Circuit (b) consists of a common-gate FET. Circuit (c) consists of a common-source FET with a feedback resistor R_f. The noise figure of circuit (a) was degraded 3–6 dB by the matching resistor. For circuits (b) and (c), noise figures were improved by increasing the gate width of the input FET's. For circuit (b), this improvement was limited because the gate width must be determined to satisfy an input matching condition. For circuit (c), the gate width was increased without any effect on the input matching condition. Therefore, the noise figure of circuit (c) was improved more than that of circuit (b) by choosing the appropriate values of the gate width and the feedback resistor. The results calculated by the computer are shown

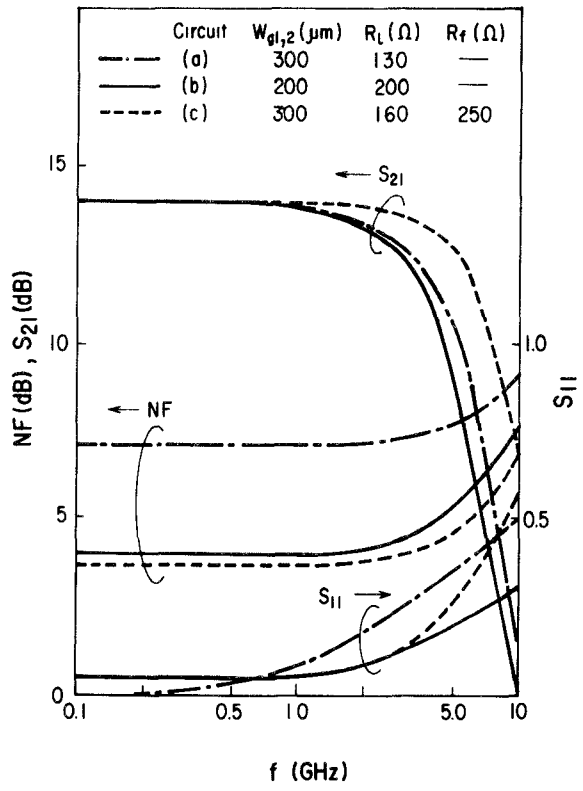


Fig. 3. Simulated frequency dependencies of transducer gain S_{21}, input reflection coefficient S_{11}, and noise figure NF for circuits (a), (b), and (c).

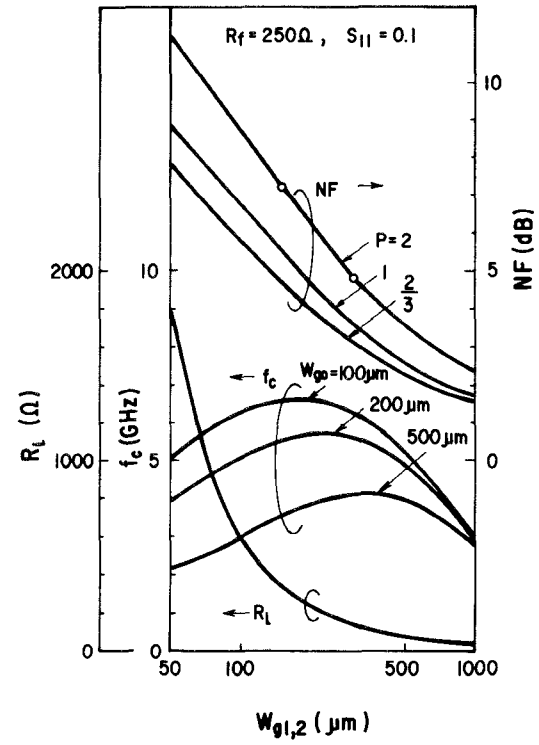


Fig. 4. −3-dB bandwidth f_c, noise figure NF, and load resistor R_1 versus the gate widths $W_{g1,2}$ of input FET and source-follower FET with an output FET gate width W_{go} as a parameter. Transducer gains are 8 dB, 13 dB, and 19 dB for 100-μm, 200-μm, and 500-μm gate-width output FET, respectively. Plotted circles represent experimental results.

in Fig. 3. In this figure, the frequency dependencies of transducer gain S_{21}, input reflection coefficient S_{11}, and noise figure NF, calculated with P of 1, were compared under the constant-S_{21} condition. The gate width of an input FET for circuit (b) was chosen to be 200 μm to obtain the input matching. Those for circuits (a) and (c) were 300 μm to lower the noise figure. Each circuit had a 200-μm wide common-source output FET for operation to an external 50-Ω load. It was found from Fig. 3 that circuit (c) was most suitable for use as a preamplifier among these circuits due to its broad bandwidth and low noise figure.

The important design factors to reduce the noise figure for this circuit were the FET gate width and the feedback resistor. Fig. 4 shows −3-dB bandwidth f_c, NF, and load resistor R_1 versus the gate widths $W_{g1,2}$ of the input FET and the source-follower FET with the output FET gate width W_{go} as a parameter. In this simulation, the feedback resistor was fixed and the load resistor was varied to keep S_{21} and S_{11} constant for each output FET gate width. NF was calculated at 1 GHz, assuming that P was 2/3, 1, or 2, and the small noise contribution of the output FET was not included. Although NF was improved by increasing the gate width, an optimum gate width to obtain the maximum f_c existed for each W_{go}. This was because f_c degraded due to the large input capacitance for large gate width and degraded due to the large load resistor, which was necessary to input matching for a small gate width. For small W_{go}, large f_c was obtained and the optimum gate width shifted to a small value because the capacitive load against the source follower was small. However, the gain to external 50-Ω load decreased for small W_{go}.

Fig. 5 shows f_c, NF, S_{11}, and R_1 versus the feedback resistor R_f under the constant S_{21} condition. Gate widths were 300 μm for the input and source-follower FET's and 200 μm for the output FET. The same assumptions given in Fig. 4 were used in the noise calculations. NF improvement in this case was less significant than that seen in Fig. 4. Moreover, f_c decreased monotonically with increasing feedback resistance due to smaller feedback value, and S_{11} was changed to keep S_{21} constant. Therefore, increasing the gate width was more effective for improving the noise figure than increasing the feedback resistor.

Based on the above results, one-stage and two-stage preamplifiers were designed as shown in Fig. 6. For the one-stage preamplifier, gate widths were designed to be 300 μm for NF below 5 dB as referred to in Fig. 4. For the two-stage preamplifier, a modified circuit with a feedback FET instead of a feedback resistor was cascaded with an interstage inductance to the one-stage preamplifier. The design of the circuit and the interstage inductance is described in the next section. The gate width of the output FET for each amplifier was chosen to be 200 μm for operation to an external 50-Ω load. S_{21} and S_{11} were designed to be 13 dB and 0.1 for the one-stage preamplifier, and 20 dB and 0.1 for the two-stage preamplifier, respectively.

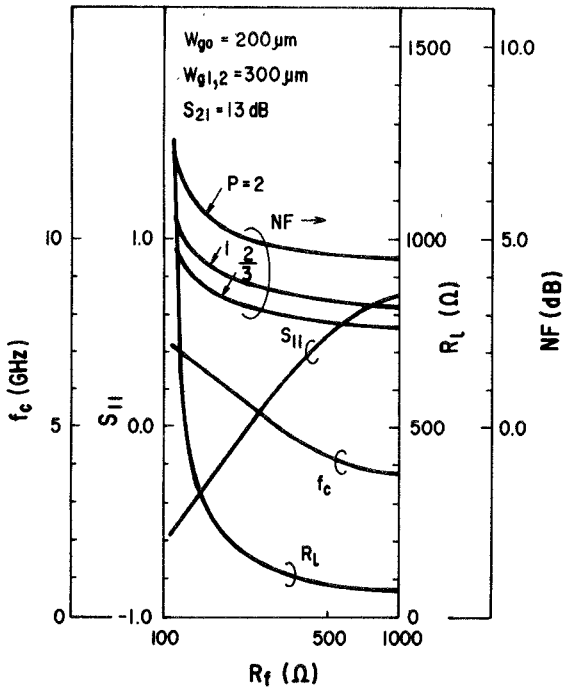


Fig. 5. −3-dB bandwidth f_c, noise figure NF, input reflection coefficient S_{11}, and load resistor R_1 versus the feedback resistor R_f.

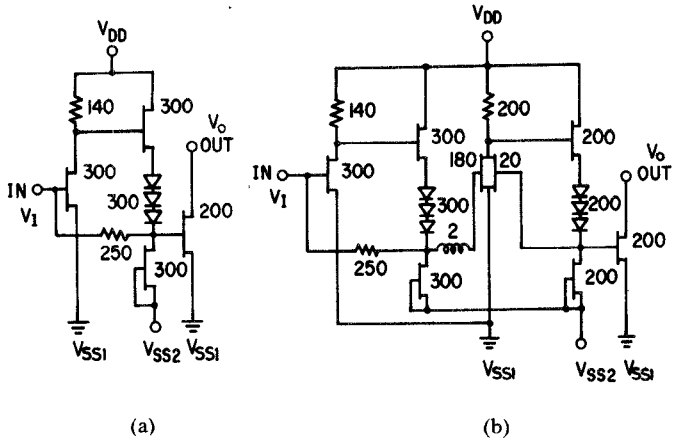


Fig. 6. Circuits of one-stage and two-stage preamplifiers. Number adjacent to each element represents FET and diode gate widths in microns, resistor values in ohms, and inductance values in nano henries.

B. The Main Amplifier

For the main amplifier, it was necessary to optimize a multistage construction to obtain high gain and broad bandwidth. Fig. 7 shows two kinds of direct-coupled circuits and their voltage gain G_v and −3-dB bandwidth f_c versus the number of amplifier stages. Circuit (a) uses only a common-source FET, and circuit (b) uses a common-source FET with a feedback FET. The gate widths for the input FET and the source-follower FET for each circuit are 180 μm and 200 μm, respectively. Circuits (b) with different gate widths for feedback FET's (20 μm for case 2 and 40 μm for case 3) were also compared (Fig. 7). Under the same gain condition, circuit (b) has a larger f_c than circuit (a). This was because the output impedance of circuit (b)

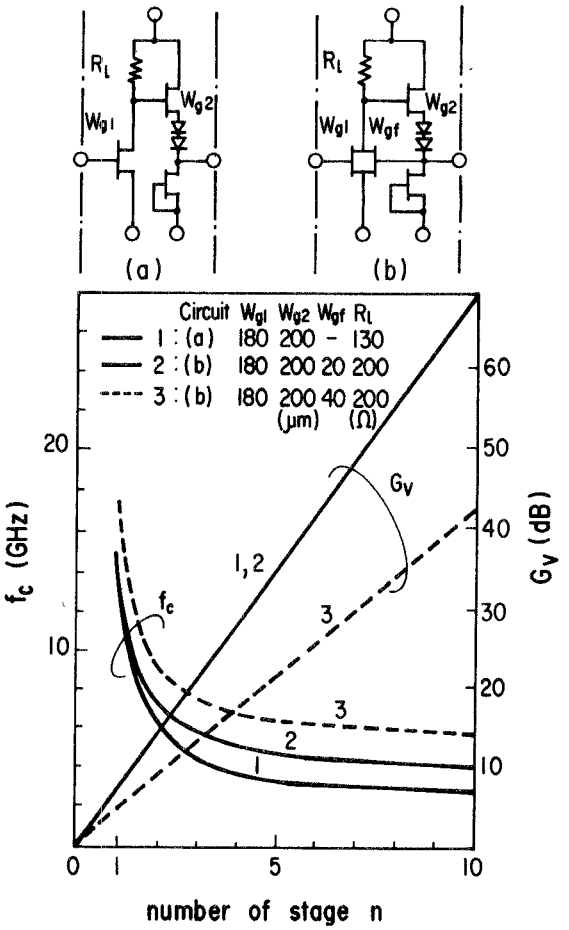


Fig. 7. Voltage gain G_v and −3-dB bandwidth f_c versus number of amplifier stages n with circuits (a) and (*b*) as unit amplifier stages.

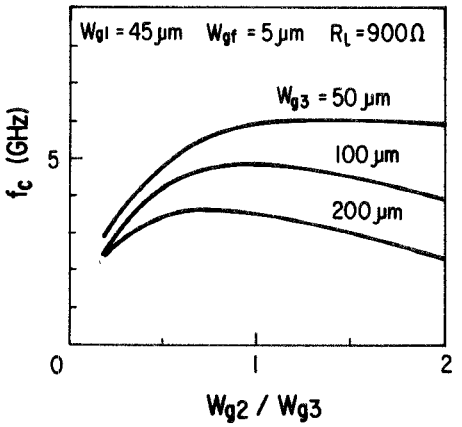


Fig. 8. −3-dB bandwidth f_c versus gate-width ratio W_{g2}/W_{g3} of a source-follower FET to a next-stage common-source FET.

was reduced by the feedback FET, and bandwidth degradation between the stages became small. Moreover, it was found from Fig. 7 that circuit (b) with the large gate width for the feedback FET had a large f_c under the same gain condition due to small output impedance. Therefore, circuit (b) was suitable for multistage construction.

For multistage construction, it was also necessary to optimize the gate width of a source-follower FET to obtain

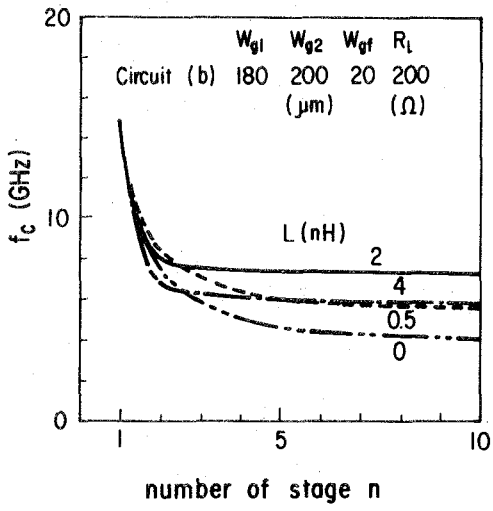


Fig. 9. −3-dB bandwidth f_c versus number of amplifier stages n with an interstage inductance L as a parameter.

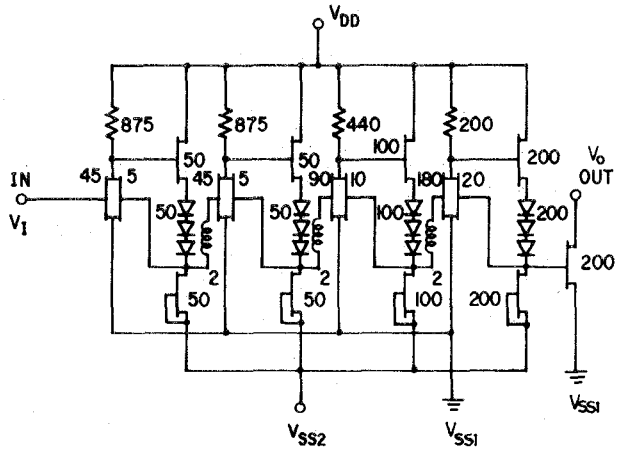
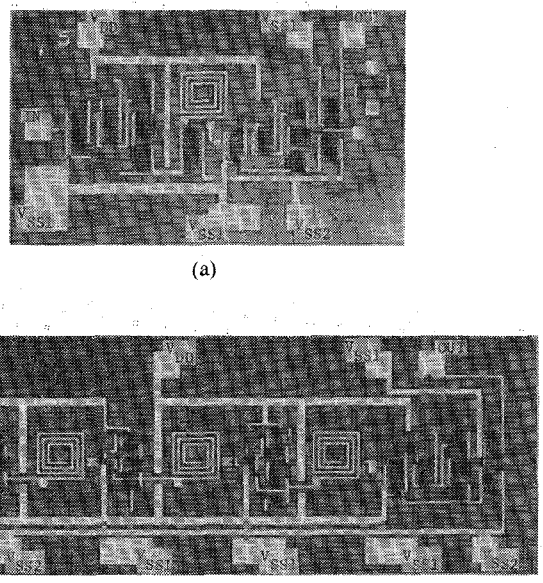


Fig. 10. Circuit of a four-stage main amplifier. Number adjacent to each element represents FET and diode gate widths in microns, resistor values in ohms, and inductance values in nano henries.



(a)

(b)

Fig. 11. Microphotographs of the developed GaAs direct-coupled amplifiers. (a) A two-stage preamplifier. (b) A four-stage main amplifier.

the broad bandwidth. Fig. 8 shows −3-dB bandwidth f_c versus the gate-width ratio W_{g2}/W_{g3} of a source-follower FET to a next-stage common-source FET. In this simulation, gate widths of input and feedback FET's were 45 μm and 5 μm, respectively. The ratio of W_{g2}/W_{g3} had an optimum value for obtaining maximum f_c for each W_{g3}. The bandwidth f_c degraded due to a large source follower input capacitance for large W_{g2}/W_{g3} and degraded due to a large output impedance for small W_{g2}/W_{g3}. For small W_{g3}, f_c degradation for large W_{g2}/W_{g3} was not significant because the capacitive load against the source follower was small.

Bandwidth was also improved by adding an interstage inductance as shown in Fig. 9. In this simulation, circuit (b) of Fig. 7 with a 180-μm-wide input FET, 20-μm-wide feedback FET, and 200-μm-wide source-follower FET was used as a unit amplifier stage and the inductance was varied as a parameter. The interstage inductance has a peaking effect due to a series resonance with the input capacitance of the next stage. To improve the bandwidth, the inductance should be chosen so that the resonance frequency is located in the neighborhood above the amplifier's −3-dB bandwidth without the inductance. In Fig. 9, the optimum value of inductance was 2 nH. For both smaller and large inductance values, f_c was degraded because the location of the resonance frequency was not appropriate.

Based on these results, a four-stage main amplifier with interstage inductances was designed as shown in Fig. 10. Total gain was aimed to be 30 dB with a power consumption of 670 mW. Gain distribution was designed to be about 7.2 dB for each stage and about 1 dB for the output FET. The gate width of an output FET was chosen to be 200 μm for operation into an external 50-Ω load. Gate widths for each stage were chosen to obtain low power consumption as well as broad bandwidth. The gate-width ratio of an input FET to a feedback FET was chosen to be 9:1, i.e., 45 μm:5 μm for the first and second stages, 90 μm: 10μm for the third stage, and 180 μm:20 μm for the fourth stage. The gate widths of the source-follower FET's were chosen as in Fig. 9, that is, to equal the sum of the source-follower and feedback FET gate widths. Interstage inductances were designed to obtain gain flatness within 3 dB. Optimization of the inductance value for each stage was not considered in this work and the same value of 2 nH was used.

IV. Fabrication

The amplifiers were fabricated by self-aligned implantation for n^+-layer technology (SAINT) [7] and the gate patterns were written directly by E-beam lithography. The details of the fabrication are described in [4] and [10]. The gate length and threshold voltage of the FET were 0.7 μm

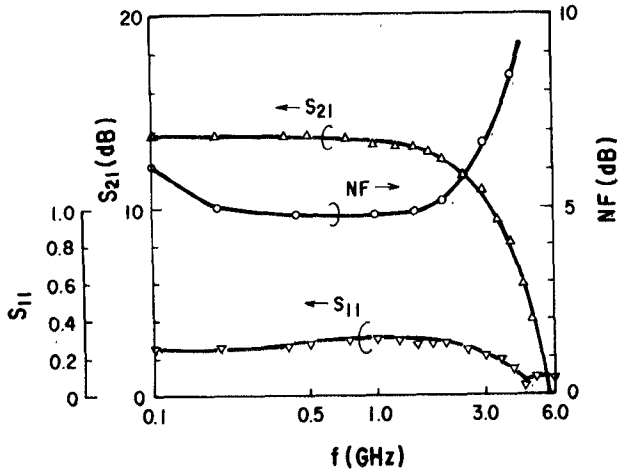


Fig. 12. Frequency dependencies of transducer gain S_{21}, input reflection coefficient S_{11}, and noise figure NF for the developed one-stage preamplifier.

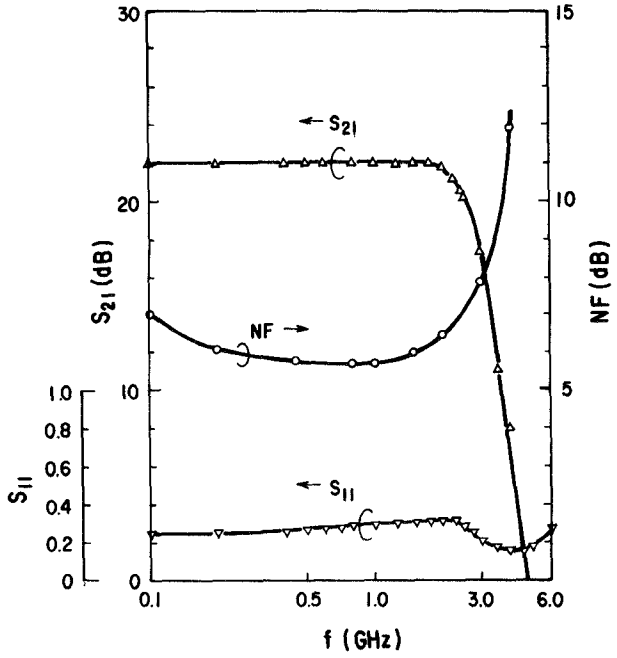


Fig. 13. Frequency dependencies of transducer gain S_{21}, input reflection coefficient S_{11}, and noise figure NF for the developed two-stage preamplifier.

and -1 V. Fig. 11 shows microphotographs of the two-stage preamplifier and four-stage main amplifier. Chip sizes of the one-stage and two-stage preamplifiers and the main amplifier were 0.8 mm $\times$ 0.8 mm, 0.8 mm $\times$ 1.2 mm, and 0.8 mm $\times$ 2.2 mm, respectively.

V. Performance

Amplifiers were mounted on a 50-Ω coplanar waveguide test fixture and their microwave performance was measured with an automatic network analyzer (HP-8545A) and an automatic noise figure meter (AIL-75).

Frequency dependencies of S_{21}, S_{11}, and NF for the one-stage preamplifier are plotted in Fig. 12. The amplifier was biased at $V_{DD} = 7$ V, $V_{ss2} = -4$ V, and $V_0 = 2$ V. The

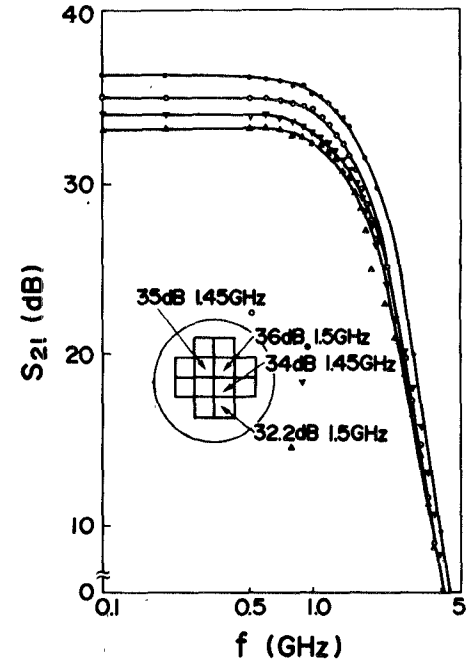


Fig. 14. Frequency dependencies of transducer gain S_{21} for four main amplifier chips and their locations on the wafer.

TABLE III
Performance of the Developed GaAs Monolithic Direct-Coupled Amplifiers

Circuit		Performance				
		S_{21}	S_{11}	f_c	NF	P
Preamplifier	One stage	14dB	0.26	3GHz	4.8dB	500mW
	Two stage	22dB	0.25	2.7GHz	5.6dB	960mW
Main amplifier		36dB	—	1.5GHz	—	710mW

S_{21}: Transducer gain. S_{11}: Input reflection coefficient. f_c: -3-dB bandwidth. NF: Noise figure at 1 GHz. P: Power consumption.

amplifier has a flat gain of 14 dB and -3-dB bandwidth of 3 GHz with a power consumption of 500 mW. S_{11} was less than 0.3 over the -3-dB bandwidth. NF had a minimum value of 4.8 dB around 1 GHz. This noise figure is plotted in Fig. 4, along with measured data from the same amplifier with 150-μm gate-width FET's instead of 300 μm. The measured relationship between NF and gate width agreed well with the calculation for $P = 2$. Gain distribution of the amplifier on the wafer was measured at 1 GHz with an RF probe card. All 12 amplifiers on the wafer operated at 1 GHz with uniform performance. Their average gain was 13.2 dB with a standard deviation of 0.45 dB.

Frequency dependencies of S_{21}, S_{11}, and NF for the two-stage preamplifier are plotted in Fig. 13. The amplifier was biased at $V_{DD} = 8$ V, $V_{ss2} = -4$ V, and $V_0 = 2$ V. The amplifier had a flat gain of 22 dB and -3-dB bandwidth of 2.7 GHz with a power consumption of 960 mW. S_{11} had nearly the same frequency dependency as that of the one-stage preamplifier. Minimum NF degraded to 5.6 dB compared to the one-stage preamplifier. This was because

the gain of the first stage was not large enough to minimize the noise contribution of the second stage.

Frequency dependencies of S_{21} for the four main amplifier chips and their locations on the wafer are shown in Fig. 14. Biasing voltages V_{DD}, V_{ss2}, and V_0 were 7 V, -4 V, and 2 V, respectively. The input biasing voltage V_I was tuned around 0.25 V within the voltage range of ± 0.1 V. Gain scattering was rather low in spite of the absence of pre-screening steps before microwave measurements. The amplifiers had flat gains of 32–36 dB and -3-dB bandwidth of about 1.5 GHz with a power consumption of 710–790 mW.

Performance of the developed amplifiers is summarized in Table III.

VI. Conclusion

The design and performance of a GaAs direct-coupled preamplifier and main amplifier was described. The developed preamplifiers had 13-dB gain, 3-GHz bandwidth, and 4.8-dB noise figure for a one-stage amplifier, and 22-dB gain, 2.7-GHz bandwidth, and 5.6-dB noise figure for a two-stage amplifier. The developed four-stage main amplifier had 36-dB gain and 1.5-GHz bandwidth with a power consumption of 710 mW. These amplifiers are promising for application to high-speed data communication systems.

Acknowledgment

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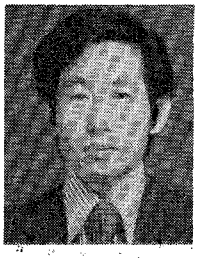

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